

COMMUNICATION DEVICE FOR TRANSMITTING MESSAGE SIGNALS

The invention relates to a communication device according to the preamble of patent claim 1.

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- Depending on the fault tolerance required of a communication device, different redundancy structures can be [sic] provided for the peripheral line assemblies belonging thereto. Examples of this are the "1+1", "1:1", and "1:N" types of line assembly redundancy, as is described in "IEEE Journal on Selected Areas in Communications" (Vol. 15, N. 5, June 1997, pp. 795-806). In a "1+1" redundancy structure, two line assemblies are operated in parallel, in order to transmit message signal currents over them redundantly. But only one of these redundant message signal currents is considered for further processing.
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- 15 In a "1+1" line assembly redundancy, only one of two line assemblies is used as the active line assembly, while a changeover onto the other line assembly, which serves as a back-up assembly, occurs only in case of a failure of the active line assembly.

- Finally, in a "1:N" line assembly redundancy, in addition to a plurality N of line assemblies, a single backup line assembly is provided. When a failure occurs on one of the N line assemblies, the backup line assembly is then used instead.
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- In a "1:N" line assembly redundancy, a selector arrangement is typically connected between the line assemblies and external transmission lines, which arrangement can distribute individual transmission lines to the N lines assemblies and to the backup line assembly. But it must be noted that, when a selector arrangement such as this fails, or respectively, in a resulting replacement of this selector arrangement, all the transmission lines that are connected to it are interrupted, along with the connections running via these lines.
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The present invention is detailed below with the aid of drawings. These drawings illustrate only those elements which are necessary in order to gain an understanding the present invention.

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Figure 1 sectional diagram of the schematic structure of a communication device according to the invention,

Figure 2 sectional diagram of the schematic structure of a coupling element that is detailed below, and

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Figure 3 the schematic structure of a control device that is provided in the coupling element illustrated in Figure 2.

The communication device KE illustrated in Figure 1 is a matter of ATM communications equipment that functions in accordance with asynchronous transfer mode, enabling the transmission of message signals in the form of message cells in the course of virtual connections. Since the ATM principle and the general structure of message cells have long been known, these are not detailed here. It is merely noted here that the message cells appertaining to a virtual connection have an information part ("user part") and a cell header ("header") at their disposal, respectively. Among other things, a cell header like this contains what is known as a virtual channel number VCI, which references the respective virtual connection, and potentially what is known as a virtual path number VPI, a routing address that applies to the respective virtual connection, and what is known as housekeeping information, as well.

The communication device KE comprises a central coupling field ASN, which has at its disposal a central coupling arrangement ASN-C (ASN Core) with an appertaining coupling arrangement control ASN-CC, and at least one ATM multiplexer AMX that is connected to the coupling arrangement. This ATM multiplexer comprises a separate control, referenced AMX-C.

The communication device KE can be a matter of what is known as a cross connect for setting up virtual permanent connections, or a switching node for setting up virtual dial connections. In either case, the set-up of the connections is accomplished with the aid of said coupling arrangement control ASN-CC and of the control AMX-C. However, since this process of setting up virtual connections is not subject matter of the present invention, it is not discussed in greater detail here.

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Figure 2 is a sectional illustration of the schematic structure of a coupling element SE for the outgoing direction of transmission. The backup switching principle just described is detailed with the aid of this Figure and Figure 3.

The logical queues Q0 to Q15 are processed – for instance, by a scanner (which is not illustrated) – cyclically in succession in a definite order, whereby one address pointer is extracted from each of the queues per cycle. Within the respective queue, the entered address pointers are read out in accordance with the FIFO principle. The address pointers that are loaded by the cell memory ZP are entered into the queues in question with the aid of a queue control QC. For this purpose, with each arrival of a message cell, this control is supplied at least with the part of the appertaining cell header in which the abovementioned routing address RA (Figure 2) is contained.

With the aid of this header, the queue into which the address pointer just loaded is to be entered is determined.

The above described controlling of the logical queues by the queue control QC is
5 discussed below in detail with the aid of Figure 3.

The central part of the queue control QC is formed by a transfer logic arrangement LPS, by means of which one or more arbitrary queues of the queues Q0 to Q15, and thus one or more line assemblies LIC A0 to LIC A15, can be randomly allocated to
10 each routing address RA. For this purpose, a register is kept in the transfer logic arrangement LPS for every routing address possibly contained in the message cells. In each of these registers, a separate bit position is reserved for each of the queues Q0 to Q15; that is, in the given example, there are 16 bit positions provided per register. The queue into which the address pointer that has been detected for a message cell is
15 to be entered during the storing of this cell is indicated by a specified logic level, for instance "1", in one or more bit positions of a register. By contrast, a logic level "0" signifies that the allocated queue is blocked.

The individual registers can be individually controlled at least according to the
20 abovementioned routing addresses RA, which are contained in the respective message
cells. The controlling is accomplished with the aid of a control logic arrangement
(which is referenced QA in Figure 3), to which the routing address that is contained in
the appertaining cell header is delivered with each arrival of a message cell.

25 Furthermore, the register contents of the transfer logic arrangement LPS are preloaded jointly by the control unit AMX-C illustrated in Figure 1 (which process is not illustrated) when the communication device KE is initialized (Figure 1), or they are modified individually if necessary; that is, in a backup switching process as described above, for example.

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When a "1+1" assembly redundancy is required, two – for instance, adjacent – bit positions in the registers of the changeover logic arrangement LPS are set to the logic level "1", respectively, in order to thereby mark the queues that are allocated to these

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